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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/866,269	05/25/2001	Sasan Cyrusian	10808/27	5524

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EXAMINER	
COX, CASSANDRA F	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/866,269	CYRUSIAN, SASAN	
	Examin r	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08/11/03* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 17-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-14 and 17-19* is/are allowed.

6)☒ Claim(s) *1,3 and 4* is/are rejected.

7)☒ Claim(s) *2,5 and 6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Applicant's arguments with respect to claims 1-4 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 is indefinite because it appears to the examiner that the applicant is trying to include a fifth and sixth transistor in a circuit which has been claimed as only containing four transistors. If the circuit is a four-transistor delay unit as called for in independent claim 1, then there can be no fifth and sixth transistor as called for in dependent claim 3. Correction or clarification is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Masaki et al. (U.S. Patent No. 5,680,064).

In reference to claim 1, Masaki discloses in Figure 2 a four-transistor differential controlled delay unit comprising: a first amplifier (TP1, TP2) having a first and second transistor connected as a two-transistor positive amplifier, wherein a gate of the first transistor (TP1) is connected to a drain of the second transistor (TP2) and a gate of the second transistor (TP2) is connected to a drain of the first transistor (TP1); and a second amplifier (TN1, TN2) having a third and fourth transistor, a drain of the third and fourth transistors connected to a drain of the first and second transistors to form output terminals (OUT1, OUT2), wherein a differential input voltage is connected to gates of the second amplifier transistors (TN1, TN2), a control input and power supply voltage (VDD2) controlling the delay (this is seen to be inherent) is connected to sources of the first amplifier (TP1, TP2) and the delay unit uses substantially all available power supply voltage. The same applies to claim 4, wherein a control input and supply voltage (GND) is connected to the sources of the second amplifier (TN1, TN2), and wherein a delay period is determined by the control input and supply voltage.

Allowable Subject Matter

6. Claims 7-14 and 17-19 are allowed.

7. Claims 2 and 5-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: Claim 2 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 5 wherein a delay line comprises at least two of the

four-transistor delay units connected in series (82, 84). Further, the closest prior art of record, Masaki, fails to disclose any motivation for substituting the converter of figure 2 as a delay unit in a voltage controlled oscillator in combination with the rest of the limitations of the base claims and any intervening claims. Claim 5 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 4A wherein the first amplifier transistors (76, 78) are NMOS transistors and the second amplifier transistors (72, 74) are PMOS transistors in combination with the rest of the limitations of the base claims and any intervening claims. Claim 6 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 4A wherein a positive supply voltage (Vpos) is connected to the second amplifier (72 and 74) and a negative supply voltage (Vneg) is connected to the first amplifier (76 and 78) in combination with the rest of the limitations of the base claims and any intervening claims.

9. The following is an examiner's statement of reasons for allowance: Claims 7-14 and 17-19 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 5 wherein a voltage controlled oscillator comprises a first delay unit (82) and a second delay unit (84), each further comprising four transistors (86, 88, 90, and 92), having the specific connections as called for in the claims. Further, the closest prior art of record, Masaki, fails to disclose any motivation for substituting the converter of figure 2 as a delay unit in a voltage controlled oscillator in combination with the rest of the limitations of the base claims and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

10. Applicant's arguments filed 02/09/04 with respect to Mizuno have been fully considered but they are not persuasive. Applicant's argument that Mizuno does not disclose a delay unit is not persuasive because the circuit of Mizuno is seen to inherently generate a delay. Further, since there is no structural difference between applicant's claimed circuit and the circuit of Mizuno, both circuits are seen to perform the same operation. However, a new reference (Masaki) showing both output terminals has been cited in place of Mizuno. The same arguments apply to the Masaki reference, since there is no structural difference between applicant's claimed circuit and the circuit of Masaki, they are seen to inherently have the same function or operation.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:30 PM and on alternate Fridays from 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

CC

May 14, 2004

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800